ABSTRACT OF THE DISCLOSURE

In a data processor which comprises a semiconductor memory device, a potential on a bit line of the semiconductor memory device is monitored at the end of a precharge, required for the semiconductor memory device, to detect an anomalous frequency of a clock applied from the outside. The anomalous frequency is detected by determining whether or not the potential on the bit line has reached a predetermined potential. When the potential on the bit line has not reached a predetermined potential, the operation of a CPU is reset.

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